# Low-Power Clocked-Pseudo-NMOS Flip-Flop for Level Conversion in Dual Supply Systems

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***Abstract*—Clustered voltage scaling (CVS) is an effective way to decrease power dissipation. One of the design challenges is the design of an efficient level converter with fewer power and delay overheads. In this paper, level-shifting flip-flop topologies are investigated. Different level-shifting schemes are analyzed and classified into groups: differential style, n-type metal–oxide–semiconductor (NMOS) pass-transistor style, and precharged style. An efficient level-shifting scheme, the clocked-pseudo-NMOS (CPN) level conversion scheme, is presented. One novel level conversion flip-flop (CPN-LCFF) is proposed, which combines the conditional discharge technique and pseudo-NMOS technique. In view of power and delay, the new CPN-LCFF outperforms previous LCFF by over 8% and 15.6%, respectively.**

***Index Terms*—Dual supply, flip-flop, level conversion, low power.**

## I. Introduction

THE system-on-chip (SoC) design will integrate hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat. All of these result in power consumption being one of the main problems in achieving high-performance design. Due to quadratic relations between voltage and power consumption, reducing the supply voltage is very efficient in decreasing power dissipation. A clustered voltage scaling (CVS) scheme has been developed in [1]. In the CVS scheme, by using low supply voltage (VDDL) in noncritical paths, i.e., placing speed insensitive gates with supply voltage VDDL, and using high supply voltage (VDDH) in speed sensitive paths, the whole system power consumption could be reduced without degrading the performance. To implement CVS scheme in a chip, a level converter must be used when a gate, which is supplied by the low supply voltage VDDL, connects to a gate that is supplied by high supply voltage VDDH. The reason is that the data or clock from a low supply voltage block cannot connect to a p-type metal–oxide–semiconductor (PMOS) in a VDDH block directly, since the PMOS cannot be shut off with low supply voltage VDDL. Notice that the dual Vdd system has an overhead, being that it needs an extra power supply line for VDDL causing an area overhead in addition to the level converter's delay and power penalty. One of the main challenges in the CVS system is to design level converters with less power and latency overhead [2] to interface low-voltage blocks with high-voltage blocks.

Different level converters have been published [3], [4]. To alleviate the delay overhead of the inserted level converter, integrating the level conversion in the flip-flop is a good choice, which results in the level conversion flip-flop (LCFF). LCFF designs appeared in [1], [5]–[8]. This paper surveys various level-shifting schemes in LCFFs and classifies them into three types: differential level-shifting scheme style, n-type metal–oxide–semiconductor (NMOS) pass-transistor style, and precharged style. We also propose a novel LCFF design with lower power consumption overhead. This paper is organized as follows. Section II reviews the published LCFFs. Section III introduces the proposed level-shifting scheme with the new CPN-LCFF. Section IV shows the simulation result and Section V concludes the paper.

## II. LCFF Survey

### A. Differential Level-Shifting Scheme

One type of LCFF uses a differential level conversion structure, where the inputs in differential cascade voltage switch logic (DCVSL) circuits [9] do not connect to PMOS at all, as can be seen in Fig. 1(a) where the low-voltage inputs do not drive PMOS $P1, P2$.

One master–slave LCFF, slave latch level-shifting (SLLS) flip-flop [Fig. 1(b)], was proposed in [1]. (Devices and signals in dotted line boxes are using VDDL; the same as in other figures.) SLLS uses a differential cascade voltage switch logic (DCVSL) style level conversion scheme in the slave latch. The clock signal and the data signal in the dotted line use low-voltage VDDL, and do not connect to the PMOS directly, which makes it suitable as a level converter.

However the SLLS flip-flop has drawbacks. There is a relatively large crossover current in the internal nodes, causing large delay and power consumption [10]. The contention is aggravated when the voltages of the clock and input are low swing. The low voltage reduces the NMOS transistor's driving ability

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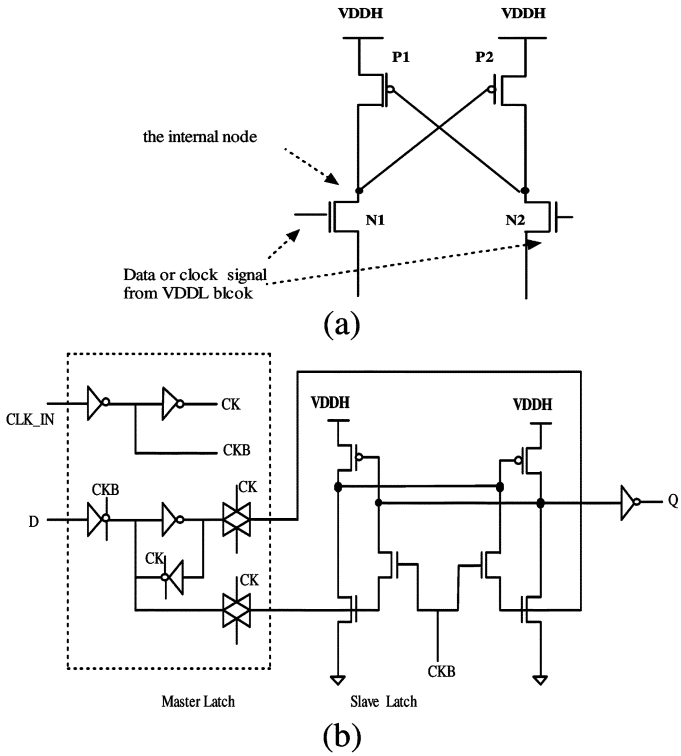


Fig. 1. (a) DCVSL level conversion scheme. (b) SLLS (devices in dotted line boxes use VDDL; the same as in other figures).

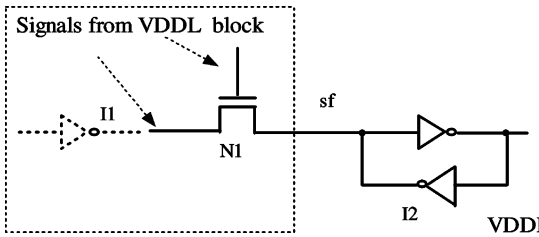


Fig. 2. NMOS level-shifting scheme.

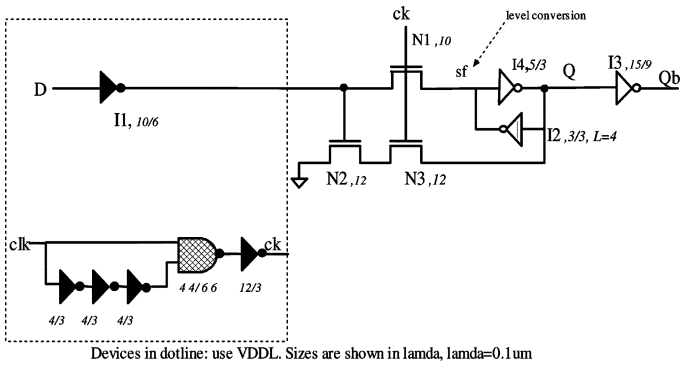


Fig. 3. Pulsed half-latch (PHL).

to pull down the internal node. The cross couple fighting between the PMOS pull-up devices and the NMOS pull-down devices is aggravated [4], which makes it difficult for this circuit to switch the logic state at transition time, therefore the delay would be larger. Moreover, it has many gates on its critical path.

Another flip-flop using differential level-shifting scheme is the clock level shifted sense amplifier (CSSA) flip-flop [1]. It consists of a sense amplifier latch [11] and set–reset latch. There is large crossover fighting that causes power consumption and delay, particularly when the clock is low swing. Moreover, CSSA uses the dynamic precharge style. If $D$ remains stable, one of the internal nodes will be charged/discharged every clock cycle, hence there is an internal redundant switching power consumption, further causing power penalty. An alternative LCFF from [7], pulsed sense amplifier (PSA), used a similar differential level-shifting scheme.

### *B. NMOS Pass-Transistor Level-Shifting Scheme*

Another level-shifting scheme is called NMOS pass transistor level-shifting scheme (Fig. 2), where one end of the NMOS transistor $N1$ connects to the low-voltage input signal, and the level shift point "$sf$" is lifted to (VDDL-Vth of the NMOS) through NMOS transistor $N1$. Keeper $I2$ will pull "$sf$" up to VDDH. One NMOS transistor $N1$ and one inverter $I2$ are used to implement the level shifting.

Pulsed half-latch (PHL) LCFF is proposed in [7] [Fig. 3 (inverters in dark use VDDL; the same as in other figures)], which uses the NMOS pass transistor level-shifting scheme. However, the data driving inverter $I1$ works at low-voltage VDDL. The keeper $I2$, which works at high voltage, fights with $I1$ during level shifting, so the keeper $I2$ cannot be too strong. Notice that there is a threshold voltage dropping due to the pass transistor $N1$; the voltage at node "$sf$" must be restored from (VDDL-Vthn) to VDDH when $D = 0$, where the difference of {VDDH-(VDDL-Vthn)} is a quite large amount. Thus, these factors negatively impact the switching significantly. The two NMOS transistors in serial $N2$ and $N3$ must be strong enough to pull $Q$ down quickly to help to lift "$sf$," but it takes a two-gate delay to do that.

One master-slave LCFF, master–slave half latch (MSHL), is proposed in [7], where the NMOS pass transistor level-shifting scheme is also used. However, it has the similar drawback of threshold voltage drop on node "$sf$" that has an impact on the speed considerably. Furthermore, it has one more gate in VDDL, resulting in larger delay than PHL as well as a slightly higher power consumption over PHL [7].

### *C. Precharged Level-Shifting Schemes*

Unlike the differential or pass-transistor level-shifting scheme, several LCFFs achieve level conversion by precharging the circuit in this scheme [Fig. 4(a)]. The precharging device will keep switching.

An elegant design, the pulse precharged (PPR) LCFF, is proposed in [7] [see Fig. 4(b)]. A low-swing clock signal drives the gate of NMOS transistor $N1$, which is connected to VDDH; when $N1$ turns on it lifts the voltage of the node $X$ to (VDDL-Vth of NMOS); PMOS transistor $P1$ in the clocked keeper will pull the node $X$ up to VDDH. However, the clocked transistors for level-converting $N1$ and $N2$ keep switching even when the input $D$ remains stable. Since this portion of power does not contribute to necessary level conversion, it causes redundant power overhead.

Another elegant level-shifting scheme is called self-precharged level-shifting scheme [6] (see Fig. 5), where

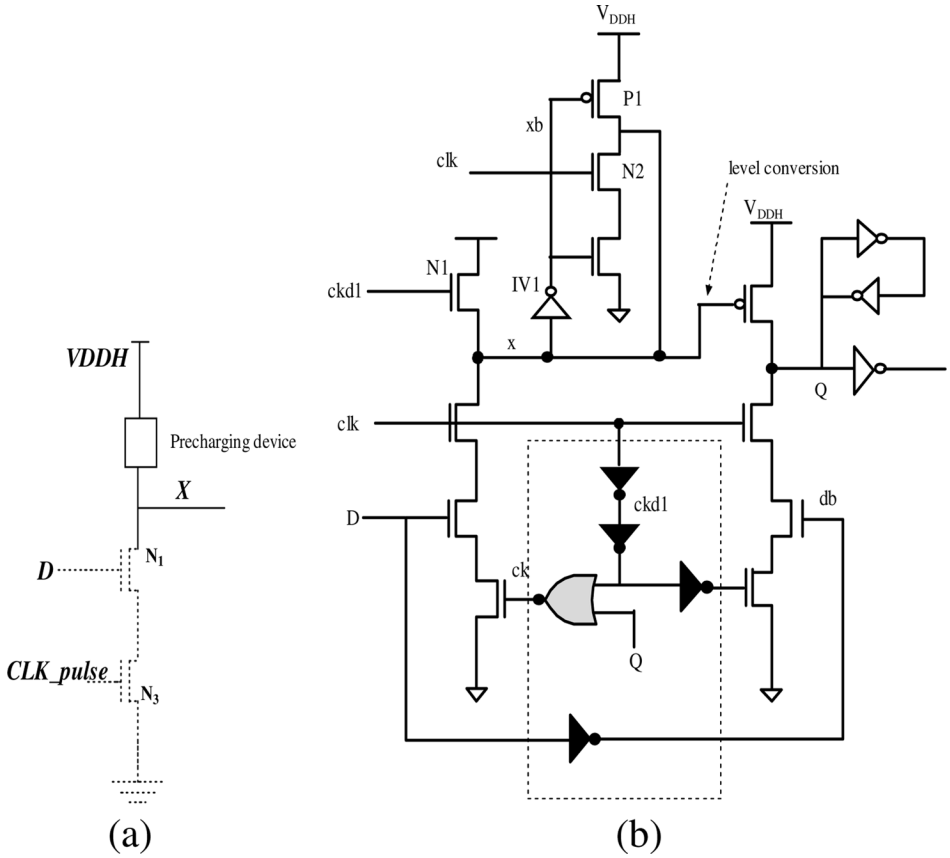


Fig. 4. (a) Precharged level-shifting scheme (precharging device will keep switching at different times). (b) PPR (the total number of the transistor: 31; clocked transistor: 13).

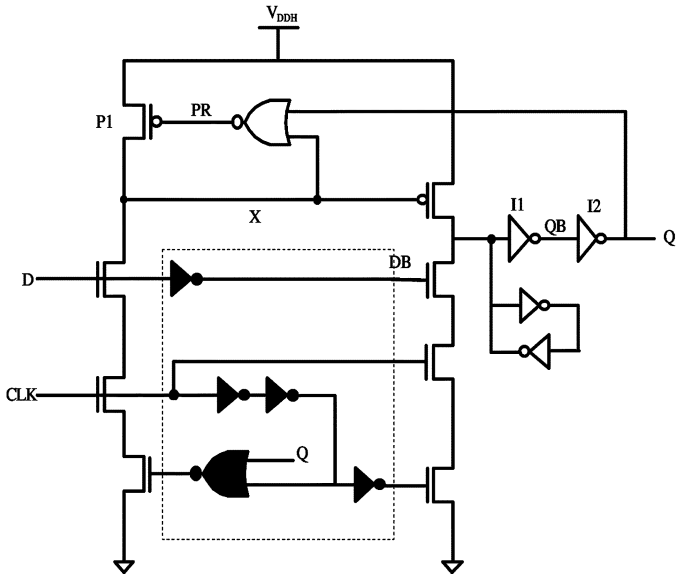


Fig. 5. SPFF (the total number of the transistors: 32; clocked transistors: 11).

the gate of PMOS $(P1)$ connects to a high voltage from a NOR gate and the last two inverters $(I1, I2)$ at the output node are employed to enable the self-precharging level-shifting scheme. However, the last two inverters $(I1, I2)$ cause delay and power consumption overhead [7].

## III. Proposed Clocked-Pseudo-NMOS LCFF

The differential level-shifting scheme normally has large delay and power overhead due to crossover contention and SLLS has larger delay and power consumption than PHL. CSSA consumes dynamic power in addition to the crossover contention problem. MSHL has larger PDP than PHL due to the long critical path (five gates) resulting in large delay, and it dissipates more power than PHL [7]. PPR dissipates more energy than PHL, thus losing its advantage in CVS systems [7]. SPFF has an overhead of the last two inverters in the critical path [7], as well as eight more transistors than PHL (a 33% increase in the number of total transistors), and it consumes more power than PHL [22]. PHL is the most efficient design in view of power consumption among LCFFs including SLLS, CSA, MSHL, PPR, and SPFF. We will not discuss SLLS, CSA, MSHL, PPR, and SPFF further in this paper due to their relatively higher power consumption than PHL.

Balanced reduction of both power and delay of an LCFF is the main method to reach improved power savings in a CVS system. PHL is the best example of this [7] in comparison with other previous designs such as PPR. However, PHL has a threshold drop problem aggravated by the low voltage of the input, and it has an explicit pulse generator, which normally consumes more power. Furthermore, it has four gates on the critical path.

To further attain power improvement, the clocked-pseudo-NMOS (CPN) level-shifting scheme is proposed [Fig. 6(a)]. In this level-shifting scheme, the PMOS $(P1)$ is always ON. This

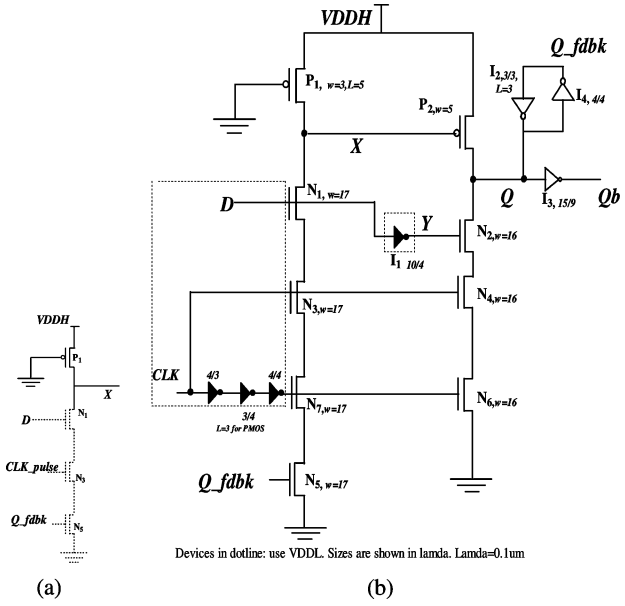


Fig. 6. (a) Proposed clocked-pseudo-NMOS level-shifting scheme. (b) Proposed clocked pseudo-NMOS level-converting flip-flop (CPN-LCFF).

scheme combines pseudo-NMOS [10] with the conditional discharge technique [13] where a feedback signal $Q\_\mathrm{fdbk}$ controls NMOS $N5$. When input $D$ stays high, $N5$ will shut off to avoid unnecessary short-circuit current as well as the redundant switching activity at node $X$. Low-swing signals including input signal $(D)$ and clock signal (CLK_pulse) are connected to the NMOS transistors $N1$ and $N3$, respectively.

A level-converting flip-flop, clocked-pseudo-NMOS level-converting flip-flop (CPN-LCFF), is proposed [Fig. 6(b)]. $Q\_\mathrm{fdbk}$ is connected to transistor N5 to disconnect discharge path when $Q = 1$ and $Q\_\mathrm{fdbk} = 0$; the second NMOS branch $(N2, N4, N6)$ is responsible for pulling down the output of $Q$.

We use a weak pull-up PMOS device $P1$ (length $L = 5$) to precharge the internal node $X$ rather than using the clocked precharge device in PPR. Although $P1$ is always ON, short circuit only occurs one time when $D$ makes a transition of $0- > 1$, and the discharge path is disconnected after a two-gates delay by $Q\_\mathrm{fdbk}$ (turning off $N5$). After that, if $D$ remains at 1, the discharge path is already disconnected by $N5$ and there will be no short circuit. This pseudo-NMOS technique is also used in [14].

$P1, N1, N3, N5$, and $N7$ should be properly sized to ensure a correct noise margin [15]. The NMOS in inverter $I4$ should not be too strong, otherwise it can disconnect $N5$ before the pulse window is closed. $P2$ should pull $Q$ up when $D = 1$, and PMOS in $I1$ should turn on $N2$ when $D = 0$. The discharge control transistor $N5$ is placed at the bottom of the NMOS stack to speed up the design, because $Q\_\mathrm{fdbk}$ is ready before the next clock edge to sample the data $D$.

The clocked-pseudo-NMOS scheme is different from the general idea of conventional pseudo-NMOS logic in that we use clocked transistors in the pull-down branch as well as a conditional discharge feedback to control transistor $N5$. Comparing this with previous published level-shifting schemes, the proposed level-shifting scheme employs only one single PMOS $P1$, resulting in an efficient design. One thing to note is that pulsed flip-flops might need more hold time than conventional flip-flops.

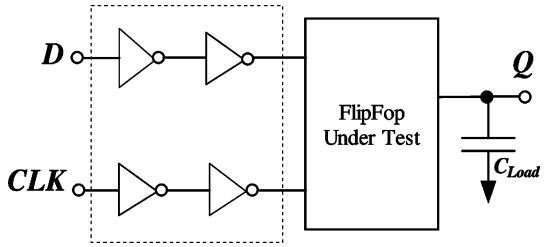


Fig. 7. Setup used for the flip-flop simulations. Inputs are driven by the inverters, and the output is driving a capacity load of 14 minimum inverters (FO14).

## IV. Simulation Results

The simulation results were obtained from HSPICE simulation in 0.18-$\mu$m complementary metal–oxide–semiconductor (CMOS) technology at room temperature. VDDH is 1.8 V and VDDL = VDDH $\times$ 70% = 1.25 V (the optimal VDDL-to-VDDH ratio is 60%-70% to yield the best power consumption [7]). The parasitic capacitances were extracted from the layouts. The setup used in our simulations is shown in Fig. 7. In order to obtain accurate results, we have simulated the circuits in a real environment, where the flip-flop inputs (clock, data) are driven by the input buffers, and the outputs are required to drive an output load. The value of the capacitance load at node $Q$ is 21 fF, which is selected to simulate a fan out of 14 minimum sized inverters (FO14) [16]. Assuming uniform data distribution, we have supplied $D$ with 16-cycle pseudorandom input data with an activity factor of 18.75% to reflect the average power consumption. A clock frequency of 250 MHz is used.

Each design is simulated using the circuit at the layout level. All capacitances were extracted from layouts such that we can simulate the circuit more accurately. This is because the internal gate capacitance, parasitic capacitance, and wiring capacitance affect the power consumption heavily in deep submicron technology. Further, the delay strongly depends on these capacitance.

Power consumed in the data and clock drivers are included in our measurements. Circuits were optimized for power–delay product (PDP). Delay is the data-to-output delay ($D$-to-$Q$ delay), which is the sum of the setup time and the clock to the output delay. The $D$-to-$Q$ delay [17] is obtained by sweeping the $0- > 1$ and $1- > 0$ data transition times with respect to the clock edge and the minimum data-to-output delay corresponding to optimum setup time is recorded. This optimization methodology is similar to that in [17] and [18].

Table I shows a comparison of the flip-flop characteristics in terms of the delay, power and power–delay–product as well as level-shifting schemes, number of transistors, number of clocked transistors, number of gates on critical path, area, and the transistor width. The waveform of CPN-LCFF when $D$ makes a $0- > 1$ transition is shown in Fig. 8.

PHL suffers from threshold voltage drop and contention problems, which are aggravated by the low-voltage VDDL of input when switching. Further, it uses an explicit pulse generator. On the other hand, CPN-LCFF uses an implicit pulse as well as it

TABLE I
Comparing the Flip-Flop Characteristics in Terms of the Delay, Power, and Power–Delay Product

| | Level shifting scheme | # of Tr. | # of clocked Tr. | # of gates on critical path | Tr. Width (um) | Area ($\lambda^2$) | DQb (ps) | P (uW) | PDP (fJ) |
|---|---|---|---|---|---|---|---|---|---|
| PHL | NMOS pass | 23 | 14 | 4 | 17.5 | 15670 | 643 | 8.29 | 5.33 |
| CPN-LCFF | Clocked Pseudo NMOS | 23 | 10 | 3 | 22.8 | 18009 | 541 | 7.61 | 4.17 |

-- Includes clocked transistors that switch with the clock both in the pulse generator and in the latch part.
-- CPN_ip, PHL use DQb as delay, respectively.
-- All the designs are implemented using layout.

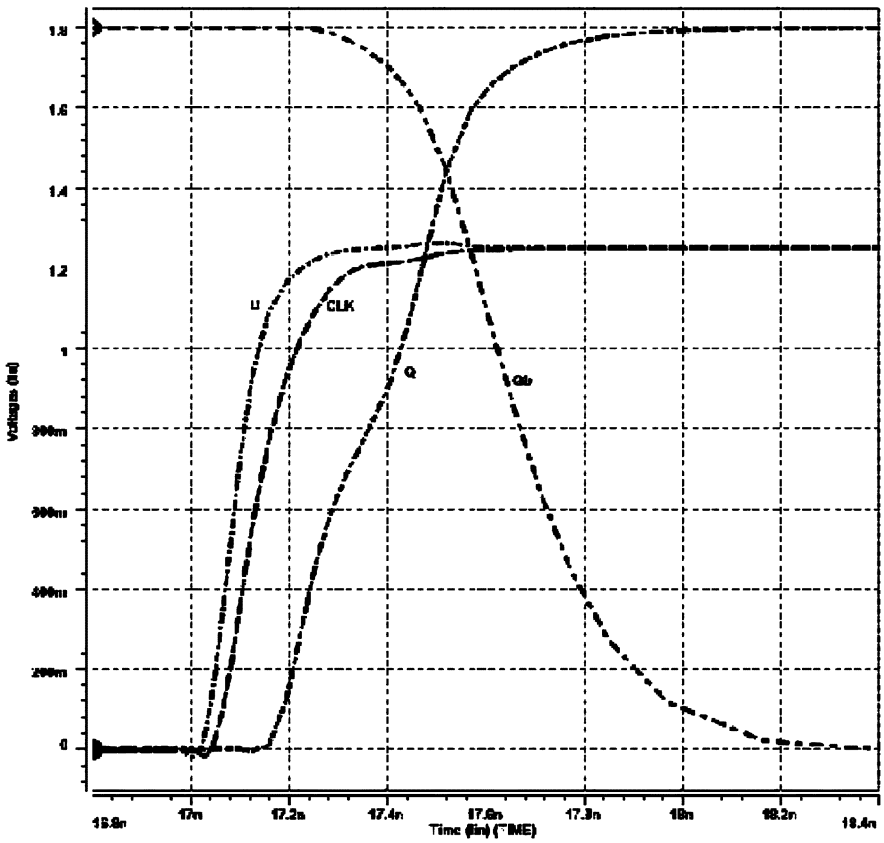


Fig. 8. Waveform of CPN-LCFF: $D0->1$ transition.

has four less clocked transistors than PHL; in addition, it has one less gate on the critical path than PHL. Hence CPN-LCFF improves power and delay over PHL by 8.2% and 15.6%, respectively. In terms of PDP, 22.7% improvement is achieved. Note that CPN-LCFF uses more areas than PHL due to up sizing of the serial NMOS transistor stacks. PHL has lower power consumption than PPR, SPFF, SLLS, CSSA, and MSHL. However, CPN-LCFF further improves power dissipation over PHL, so it is suitable to be used in low-power systems.

In view of the level-shifting scheme, the proposed clocked-pseudo-NMOS level-shifting scheme is more efficient than the other approaches such as the DCVSL style, the NMOS pass-transistor scheme, and the precharged schemes.

The clocked-pseudo-NMOS technique in combination with the conditional-discharge technique could be used on other flip-flops like ip-DCO [18], single-transistor-clocked flip-flop [20], etc., as well, because replacing the precharging clocked transistor with a pseudo-NMOS transistor (a weak always-on-PMOS) will gain power improvement.

CPN-LCFF presents small delay; besides level-shifting environment, it could also be used in a critical path (VDDH blocks in CVS systems) directly, which may simplify the structure of the dual voltage system. Further, in case of the low-swing clock system, CPN-LCFF could be used since clock signals only connect to NMOS transistors $(N3, N4, N6, N7)$.

As CMOS technology continues scaling, integrated circuits are more susceptible to soft errors and soft-error-tolerant techniques can be used [21]. With feature size shrinking, the leakage current increases rapidly and the multitreshold metal–oxide–semiconductor (MTMOS) technique can be used

to reduce leakage power consumption [5], [22]. In addition, with technology scaling, process variation tolerant techniques such as combinations of adaptive body bias and adaptive VDD may be used to reduce the variation in frequency of fabricated dies [23].

## V. Conclusion

In this paper, previous LCFFs are surveyed and their level-shifting schemes are analyzed. A novel level-shifting scheme, clocked-pseudo-NMOS scheme, is proposed. A clocked-pseudo-NMOS level-converting flip-flop is introduced, which uses the clocked-pseudo-NMOS technique.

CPN-LCFF combines the clocked-pseudo-NMOS technique with the conditional-discharge technique, and it uses an implicit pulse. In terms of power and delay, CPN-LCFF improved by 8.2% and 15.6% over PHL, respectively. In view of PDP, CPN-LCFF outperforms PHL by 22.7%. Hence, CPN-LCFF is suitable for low-power high-performance systems.

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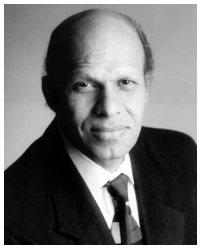

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