Low-Power Clock Branch Sharing Double-Edge Triggered Flip-Flop

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***Abstract*—In this paper, a new technique for implementing low-energy double-edge triggered flip-flops is introduced. The new technique employs a clock branch-sharing scheme to reduce the number of clocked transistors in the design. The newly proposed design also employs conditional discharge and split-path techniques to further reduce switching activity and short-circuit currents, respectively. As compared to the other state of the art double-edge triggered flip-flop designs, the newly proposed CBS_ip design has an improvement of up to 20% and 12.4% in view of power consumption and PDP, respectively.**

***Index Terms*—CMOS, double edge, flip-flop, low power.**

I. Introduction

THE CLOCK system, which consists of the clock distribution network and timing elements (flip-flops and latches), is one of the most power consuming components in a VLSI system [1]–[5]. It accounts for 30% to 60% of the total power dissipation in a system [6]. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed.

Voltage scaling is the most effective way to decrease power consumption, since power is proportional to the square of the voltage. However, voltage scaling is associated with threshold voltage scaling which can cause the leakage to increase exponentially [3].

Besides supply voltage scaling, double-edge clocking can be used to save half of the power on the clock distribution network. The $\text{power of the clocking system} = P_{\text{clock\_distribution network}} + P_{\text{flip-flop}}$. Cutting the frequency of the clock by one half will halve the power consumption on the clock distribution network.

In view that most double-edge flip-flops (DEFF) are developed from single-edge designs (SE), a brief review of SE topology is as follows. There is a wide selection of flip-flops in the literature [1]–[18]. Many contemporary microprocessors selectively use master–slave and pulsed-triggered flip-flops [3]. Traditional master–slave single-edge flip-flops [7]–[9]are made up of two stages, one master and one slave. Another edge-triggered flip-flop is the sense amplifier based flip-flop, SAFF [10]. All of these hard edged-flip-flops are characterized by a positive setup time, causing large D-to-Q delays. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. 95% of all static timing latching on the Itanium 2 processor use pulsed clocking [11]. Pulse triggered flip-flops could be classified into two types: the implicit pulse-triggered flip-flops [12]–[14]and the explicit pulse-triggered flip-flops [14]–[16].

Explicit-pulsed flip-flops (ep-FF) and implicit-pulsed flip-flops (ip-FF) have different features. First, ep-FF can have the pulse generator being shared by neighboring flip-flops, a technique that is not straightforward to utilize in ip-FF. This sharing can help in distributing the power overhead of the pulse generator across many explicit-pulsed flip-flops. Pulse generators are shared in the Itanium Processor [11]. Second, ep-FF could have the advantage of better performance since the height of the nMOS stack in ep-FF is less than that in the ip-FF [3]. However, ep-FF cannot be used with dynamic logic.

This paper is organized as follows. Section II surveys the previous published DE art and classifies them into three groups. Section III presents the new proposed clock branch sharing DEFF, and Section IV presents simulation results. Section V concludes the paper.

II. Techniques for Implementing Double Edge Triggered Flip-Flops

We survey the previous art of DEFF and categorize them into three groups: conventional DEFF, explicit pulsed DEFF, and implicit pulsed DEFF. For these three categories, we analyze the clock pulse generating scheme as well as the data latch scheme.

The DEFF design will use more clocked transistors than SEFF design generally. However, the DEFF design should not increase the clock load too much. The DEFF Design should aim at saving energy both on the distribution network (by halving the frequency) and flip-flops. It is preferable to reduce circuits' clock loads by minimizing the number of clocked transistors [1]. Furthermore, circuits with reduced switching activity would be preferable. Low swing capability is very helpful to further reduce the voltage on the clock distribution network for power saving, if applicable. Due to the fact that voltage scaling can reduce power efficiently, the cluster voltage scaling (CVS) systems are widely used. This indicates that flip-flops

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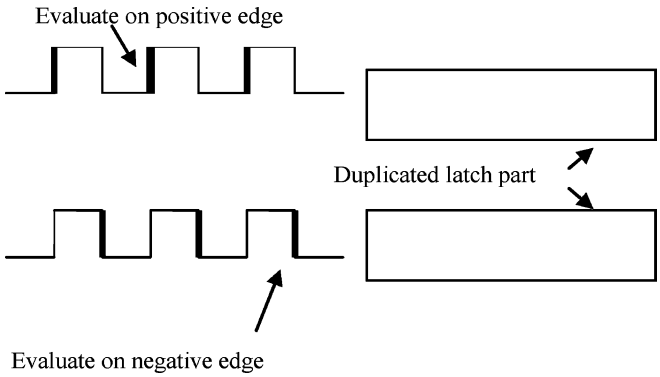

Fig. 1. General scheme for conventional dual-edge flip-flop.

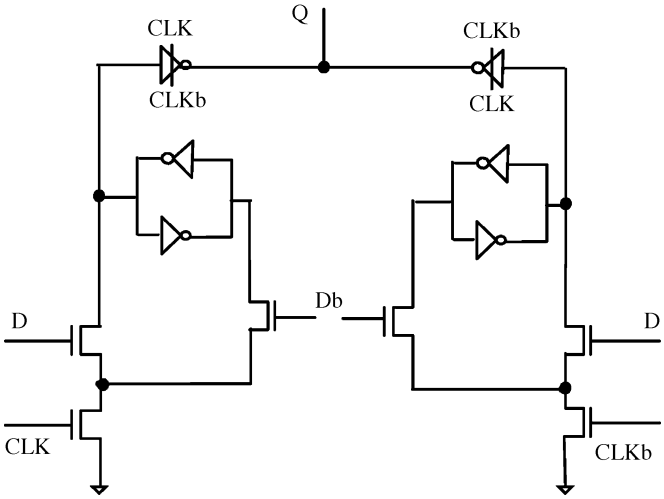

Fig. 2. Conventional dual-edge flip-flop.

with level converting ability could be used in such situations. So, integrating the level shifter with the flip-flop is helpful.

A. Conventional Master–Slave Double-Edge Triggered Flip-Flop

The general scheme is shown in Fig. 1. The conventional way of designing DEFFs is to duplicate the latch part of the single edge flip-flop to achieve sampling input data at both clock edges. This approximately duplicates the area, and also increases the load on the data and the clock inputs, which affects performance [14]. This also negatively affects (reduces) the savings gained from halving the clock frequency on the distribution network. Conventional DEFFs include [18]–[20]. One example of the conventional DE flip-flop [18]is shown in Fig. 2. The left branch samples data when $\mathrm{clk} = 1$, the right branch samples date when $\mathrm{clkb} = 1$. The data path is duplicated.

B. Flip-Flops With Explicit Pulse Generator Schemes

The master–slave FF has the hard edge property. Pulsed flip-flops allow cycle stealing and are skew tolerant. Explicit DEFFs [14], [21]–[23]use a pulse generator outside the latching part; the data latch part does not need duplication. A general scheme is shown in Fig. 3. The double-edge pulse generator could be classified as an XOR using a floating inverter (pMOS, nMOS pair that does not have a direct connection with V_{dd} or ground), an

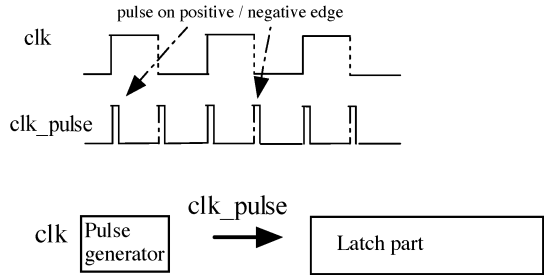

Fig. 3. General scheme of explicit pulsed DEFF.

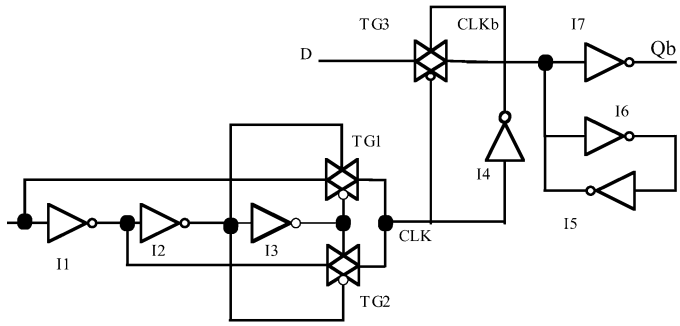

Fig. 4. Dual-edge static hybrid flip-flop (ep-DSFF).

XOR using pass transistors, or an XOR using transmission gate schemes. The latching part could be transmission gate (TG), PASS, TSPC-SPLIT, etc.

The schematic diagram of the explicit-pulsed dual-edge triggered static hybrid flip-flop (ep-DSFF) [14]is shown in Fig. 4. This design achieves a transparency window through an explicitly generated pulse. The pulse generator is elegantly designed based on TG–based XOR logic. The design has a simple structure on the critical path, so it may have less capacitive load on the critical path.

However, it has an exposed diffusion input which is subject to noise and ep-DSFF has a ratio issue [1]. An inverter may be added to the input of the TG3 to improve the driving ability and robustness.

C. Flip-Flops With Implicit Pulse-Generator Schemes

Implicit pulsed DE flip-flops [24], [25]use two series devices embedded in the logic branch receiving a clock and a delayed clock, respectively. A general scheme is shown in Fig. 5. The latching part could be TSPC-SPLIT or TSPC.

1) Symmetric Pulse Generator Flip-Flop (SPGFF): The SPGFF is shown in Fig. 6. This design achieves dual-edge triggering with two symmetric stages. Each stage responds to one particular transition of the clock, hence, the name symmetric pulse generator flip-flop [25].

Two stages X and Y of the flip-flop, shown in Fig. 6, work in opposite phases of the clock; when the clock rises, node Y is going to be charged and node X holds the value captured at the rising edge; when the clock is low, node X is precharged and Y holds the value captured at the falling edge. SPGFF needs five clock phases to ensure a correct sampling window.

The critical path of the SPGFF is to sample the D to Q $1- > 0$ transition at the CLK rising edge. If during the previous CLK1

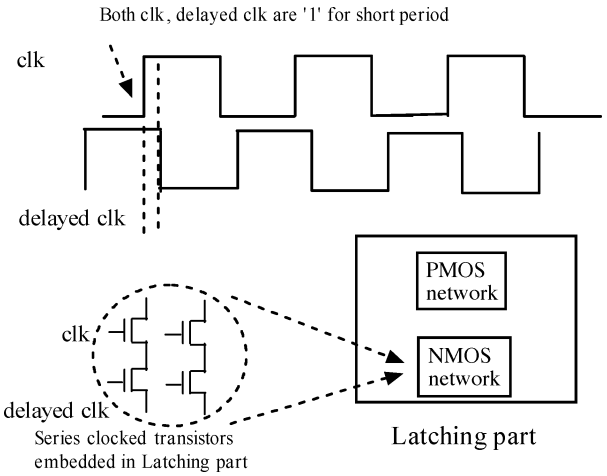

Fig. 5. General scheme of implicit pulsed DEFF.

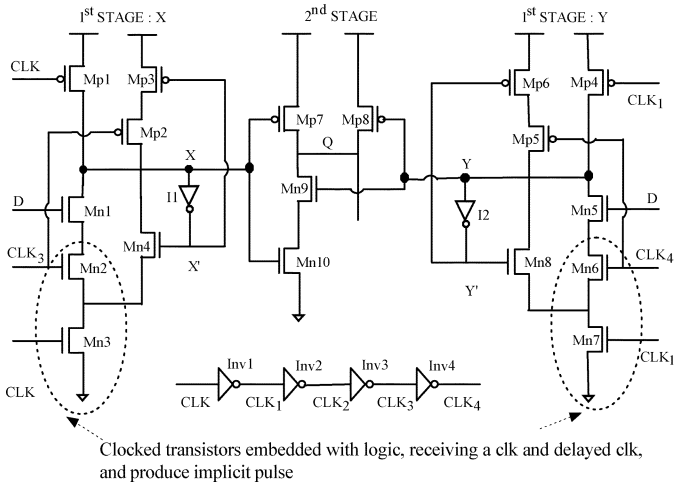

Fig. 6. Symmetric pulse generator flip-flop (SPGFF), total of 32 transistors including 16 clocked transistors.

rising edge, $\mathrm{D}=1$ and Y is discharged to 0, then D drops to 0; afterwards when CLK rises, CLK1 falls and begins to charge Y. Mp4 outputs a 1 to the NAND. At this point, the NAND has both $\mathrm{X}=1$ and $\mathrm{Y}=1$ as inputs. Following that, the NAND's output drops to 0 for a total of 3 gate delays (INV1, MP4, NAND).

Since SPGFF has two symmetric stages, it creates a separate internal node on each stage in the critical path. In addition, redundant switching exists in these nodes. When an input has a lower probability, for example if D stays at 1, node X and Y continually charge and discharge, respectively; the associated nodes X' and Y' (inverter output of X and Y) switch accordingly. These switchings consume power but do not produce anything useful; hence, they are redundant switching activities. This increases the overall power consumption since there are four redundant nodes.

Due to the dynamic nature of each stage, if D changes from "1" to "0" after evaluation begins, neither internal node X nor Y can be pulled up, therefore, this $\mathrm{D1}->0$ transition will not be evaluated during the current clock cycle.

Glitches exist at the output [25]; because of this, caution must be taken when driving the next logic gate to avoid noise propagation.

2) Double-Edge Conditional Precharge Flip-Flop (DECPFF): The DECPFF [25], Fig. 7, includes an implementation of the conditional precharge technique. Signal Q is used as a feedback signal to control precharging to reduce redundant switching activity. When D remains at 1, Q also remains at 1, thus disconnecting the precharge path by turning off P1. It uses the clocked branch separating/duplicating scheme. The nMOS clocked transistors of the 1st branch are the same structure as the nMOS clocked transistors of the second branch (in circles in Fig. 7). Both branches of the nMOS clocked transistors receive exactly the same clocks (CLK, CK, and CKD). However, the two clock branches work separately. Since it has a complex clocking structure and a large number of transistors that switch with the clock, the benefit of reducing redundant switching activity is somewhat offset by the large clocking power.

While SPGFF has a total of 16 clocked transistors (including those in the pulse generator and those embedded in the logic),

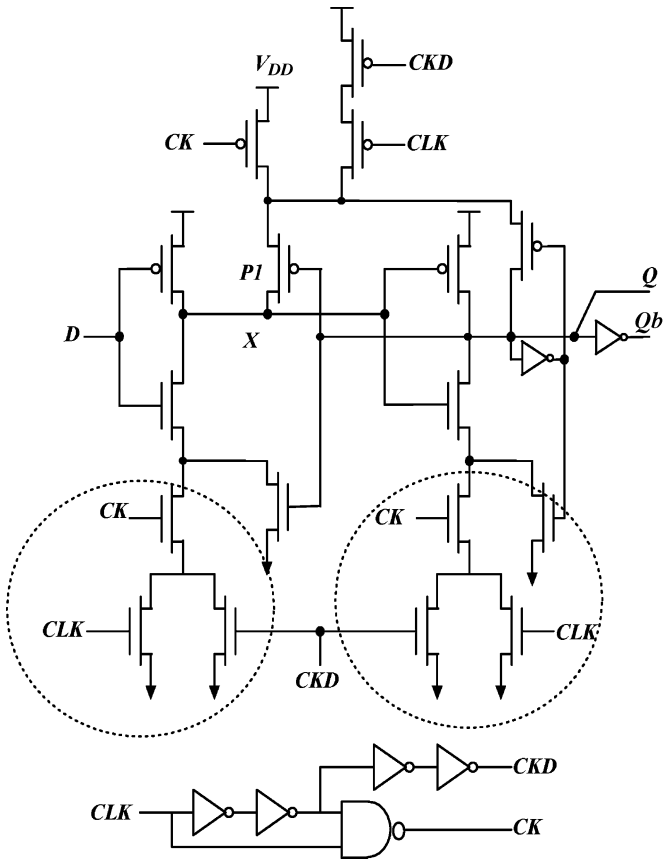

Fig. 7. Double edge conditional precharge flip-flop, total of 33 transistors including 21 clocked transistors.

DECPFF has 21 clocked transistors; its total number of transistors is 33, one more than SPGFF. The complex structure as well as the large number of clocking transistors increase the clock load and power consumption. In view of how to implement double-edge clocking, SPGFF uses five (21-16) clocked transistors less than DECPFF, thus, it is more efficient than DECPFF. We will not discuss DECPFF further in this paper.

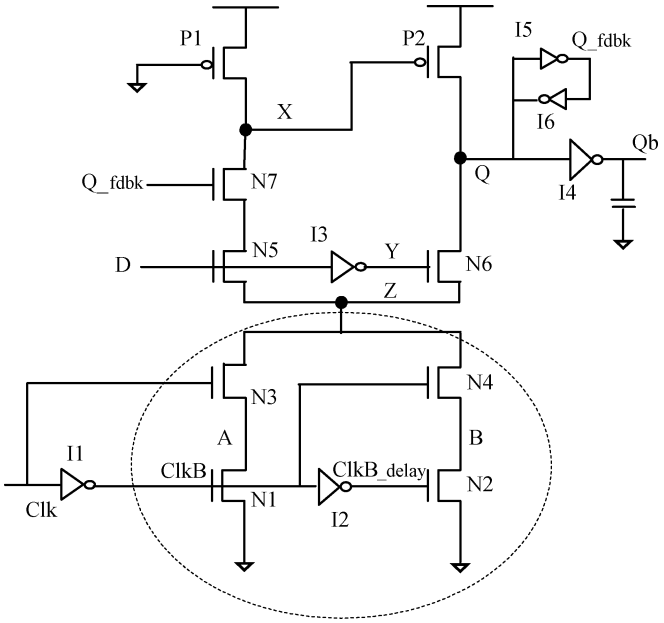

Fig. 8. Proposed CBS_ip flip-flop.

III. Proposed DE Clock Branch Sharing Implicit Pulsed Flip-Flop (CBS_ip)

Conventional DEFFs duplicate the area and the load on the inputs. Explicit pulsed DEFFs use external clock pulse generators, which increase the power. In addition, explicit pulsed DEFFs cannot work with dynamic logic. SPGFF uses implicit pulsing; however, it has four internal redundant switching nodes. Unlike SPGFF, DECPFF eliminates the redundant switching activity, however, the number of clocked transistors reaches 21, and the clock branch duplicating structure is complex.

To ensure efficient implementation of double-edge clock triggering in an implicit pulsed environment and to overcome the problem with previous implicit pulsed flip-flops which is the large clock load, a novel clock branch sharing topology is proposed. The sharing concept is similar to the single transistor clocked FF [26]and another clock branch sharing flip-flop [27]. In this new clock branch sharing scheme, Fig. 8, the two groups of clocked branches in the previous clock branch seperating scheme (DECPFF, Fig. 7) are merged; (N1, N3), (N2, N4) are shared by the first stage and second stage (in the doted circle). Note that a split path (node X does not drive nMOS N6 of the second stage, which is in the output discharging path) is used to ensure correct functioning after merging. The advantage of this sharing concept is reflected in reducing the number of transistors required to implement the clocking branch of the double-edge triggered implicit-pulsed flip-flops. Without this sharing, the number of clocked transistors would be much larger than the number of transistors used with the sharing concept. Recall that clocked transistors have a 100% activity factor and consume a large amount of power. Reducing the number of clocked transistors is an efficient way to decrease the power [1].

Using Pseudo nMOS (always on pMOS P1) in CBS_ip takes advantage of the fact that D and Qb have inversed polarity resulting from the conditional discharge technique. The discharging path only stays ON for a short while, yielding only a little short circuit current. An inverter is placed after Q, providing protection from direct noise coupling [14].

The double edge triggering operation of the flip-flop, Fig. 8, is as follows. Q_fdbk is used to control N7. When CLK rises, CLKB will stay high for a short interval of time equal to one inverter delay. During this period, the clocked branch (N1 and N3) turns on and the flip-flop will be in the evaluation period. Note that the other clocked branch (N2 and N4) is disconnected. When CLK falls, CLKB will rise, and CLKB_delay will stay HIGH for one inverter delay period during which the transistors N2 and N4 are both on, and the flip-flop is in the evaluation mode. The first stage in the design is responsible for capturing $0- > 1$ input transitions of D. The internal node X will discharge causing the outputs Q and Qb to be HIGH and LOW, respectively; N7 turns off by $\mathrm{Q\_fdbk} = 0$; If the input D stays "1," the first stage is disconnected from ground in the later evaluations preventing node X from experiencing redundant switching activity. The second stage, on the other hand, is responsible for capturing the $1- > 0$ input transitions. In this case, the falling transition of the input will cause the pull down network of the second stage to be ON and, thus, forcing the output nodes Q and Qb to be 0 and 1, respectively.

Using a split path in CBS_ip (P2 is driven by X, N2 by Y, respectively), the capacitance on node X is much smaller than that on node Q, which causes a significant difference in propagation delay through the FF. The reason for this is that node X only drives one device, P2. To further reduce latency, clocked inverters I1 and I2 are placed to drive bottom clocked transistors N1 and N2, respectively. Before the clock rising/falling edge, the output of I1/I2 turns on N1, N2, respectively, thus, the internal nodes A and B are discharged to ground before evaluation correspondingly, and this can reduce the discharge time. Though it has four stacked transistors in the first stage, the above methods (split path, and moving the early signals near GND) help to reduce the high stack's negative effect on delay.

Using the conditional discharge technique, Q_fdbk turns off N7 in two gate delays, so we need not use a 3-inverter delay in the clock pulse window. The one inverter window width is sufficient for node X to discharge to ground. The reasons are as follows. First, node X has a much smaller capacitive load than that at Q. Further, we can adjust the one-inverter-delay by weakening the nMOS in I1 and I2. Note that the nMOS in I2 and I1 control the gate of N1 and N2. Weakening of the nMOS can be achieved by using the width $(\mathrm{W}) = 3$, and increasing the length (L) of the nMOS (since the resistance is proportional to L/W). So, when L increases, the resistance increases. This allows N1 and N2 to stay ON longer after the clock rising/falling edge, respectively, before being turned off by the nMOS in I1 and I2, thus, enlarging the pulsewidth.

For the four stacked transistors, N5, N1, N3, and N7, charge sharing may occur when three of them become ON at the same time. A properly sized always-ON pMOS P1 enables a constant charging path, which reduces the effect of charge sharing. P1, N1, N2, and N3 should be properly sized to ensure a correct noise margin; the value of VOL should be small [28].

In summary, the clock-sharing scheme reduces the number of clocked transistors. The reduction of the number of clocked transistors reduces the switching activity, decreasing the power

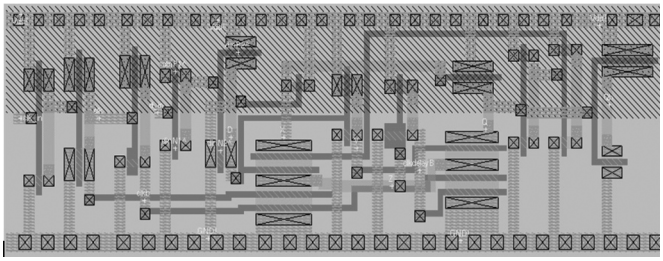

Fig. 9. One layout of CBS_ip.

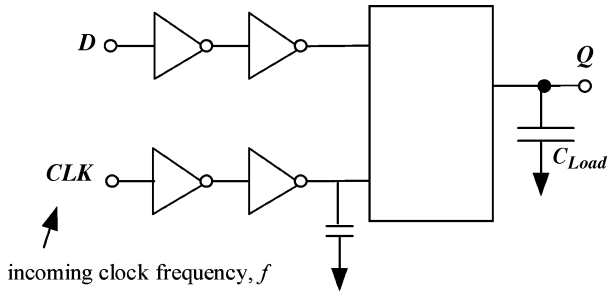

Fig. 10. Setup used for simulation.

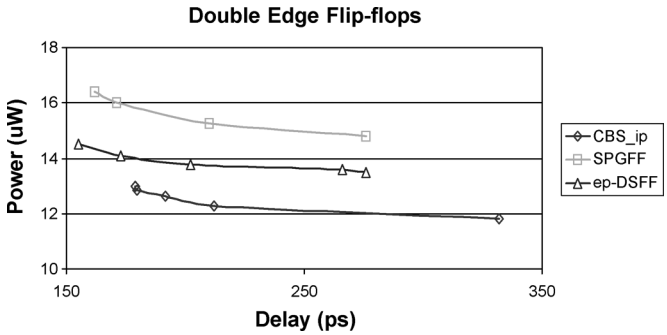

Fig. 11. Power delay curves.

usage. Also, the pseudo-nMOS replaces the pMOS clocking scheme. In addition, the conditional discharge technique and split path technique are used to reduce redundant switching activity at node X and reduce the short circuit power consumption, respectively.

IV. Simulation Results

The simulation results were obtained from HSPICE simulations in 0.18-μm CMOS technology at room temperature. Each design is simulated using the circuit at the layout level. In deep submicron technology, delay strongly depends on the internal gate capacitance, parasitic capacitance, and wiring capacitance. Further, the capacitance affects the dynamic switching power and the short circuit power as well. All capacitances that are greater than 0.0 fF were extracted from layouts, such that we can simulate the circuit more accurately.

For the CBS_ip layout, Fig. 9, we used a vertical orientation [29]when laying out the nMOS transistors in the first stage and second stage, resulting in an efficient layout, which matches the nMOS of the first stage and the second stage in the schematic.

Modern CMOS logic style has a typical activity factor of about 0.1, while the clocks have an activity factor of 1 [1], [14]. To fairly reflect all the number of transistors that switch with the clock, in this paper we consider 100% switching activity transistors as those transistors in the clock pulse generator as well as those within the logic branch that are directly driven by the clock signals.

The setup used in our simulations is shown in Fig. 10. In order to obtain accurate results, we have simulated the circuits in a real environment, where input buffers drive the flip-flop inputs (clock and data), and the outputs are required to drive an output load. The value of the capacitance at the load at Q is 21 fF (CBS_ip and ep-DSFF have their load at Qb). An additional capacitance is placed after the clock driver in the amount of 3 fF. Assuming uniform data distribution, we have supplied input D with pseudorandom input data with an activity factor of 18.7% to reflect the average power consumption [2], [30]. Power consumed in the data and clock drivers are included in our measurements. The clock frequency was 125 MHz.

Delay is measured from data D to output Q (except for CBS_ip and ep-DSFF, where delay is measured from D to Qb). Delay is the sum of the setup time plus CQ delay [1], [2]. The D-to-Q delay [30] was obtained using a similar technique as introduced in [14]. Minimum D-to-Q delay is an appropriate metric for flip-flops because it reflects the correlations between D-to-Clock delay, Clock-to-Q delay, and the D-to-Q delay.

Circuits were optimized for minimum power delay product (PDP). The D-to-Q delay is obtained by sweeping the LOW-to-HIGH and HIGH-to-LOW data transition times with respect to the clock edge, and the minimum data to output delay corresponding to optimum setup time is recorded [14]. Since both clock edges are used to sample data in DEFF, four cases of DQ are checked: sweep the high to low data transition, the same way as [14], with respect to the clock rising edge/falling edge, respectively; then sweep the low to high data transition with regard to the clock rising/fall edge, respectively, too. The worst case DQ delay is recorded. The HSPICE built in optimization capability is used in finding the minimum DQ.

For a fair comparison, we present the power versus delay curve. Fig. 11 shows the curve of power consumption at different minimum D-to-Q propagation delays for the flip-flops: CBS_ip, SPGFF, and ep-DSFF. We recorded the D-to-Q delay in the range of 150 to 350 ps to plot the curve. The transistor sizes increase while the delay decreases. This results in a plot of the power versus delay curve. Power is reduced in the case of CBS_ip by about 20% over SPGFF at the target D-to-Q delay of 170 ps. In view of PDP, the CBS_ip improved 12.4% over SPGFF.

Table I presents the comparison between the SPGFF, ep-DSFF, and the newly proposed CBS_ip. We analyze different designs in view of PDP, DQ delay, power, low swing driving ability, total transistor width, area, CQ delay, setup time, and leakage power. A waveform of D making a $0- > 1$ transition is shown in Fig. 12.

SPGFF suffers from large power consumption because of the large number of the nodes switching with the clock. Since the CMOS logic style has a typical activity factor of about 0.1, the clocks have an activity factor of 1 [1], [14]. Further, there are

TABLE I
COMPARING THE FLIP-FLOP IN TERMS OF DELAY, POWER, AND POWER DELAY PRODUCT

Design Name	# of tr	100% switching activity tr $*^1$	Area λ^2	Total transistor width (um)	Low Swing	Leakage (uw)	CQ (ps)	Setup (ps)	DQ (ps) $*^2$	Power (uW)	PDP (fJ) $*^3$
SPGFF	30	16	35148	29	N	0.905	128	35	162	16.4	2.66
ep-DSFF	20	14	25571	15	N	0.73	295	-158	155	14.5	2.25
CBS_ip	23	8	29700	22.2	Y	0.667	135	43.9	179	13.0	2.33

$*^1$ Includes clocked transistors that switch with the clock both in the pulse generator and in the latch part.
$*^2$ CBS_ip and ep-DSFF use DQb, CQb, respectively.
$*^3$ ep-DSFF has an exposed input diffusion susceptible to noise [1], if one inverter is added at the input, its PDP would degrade.
$*$ All the designs are implemented in layout.

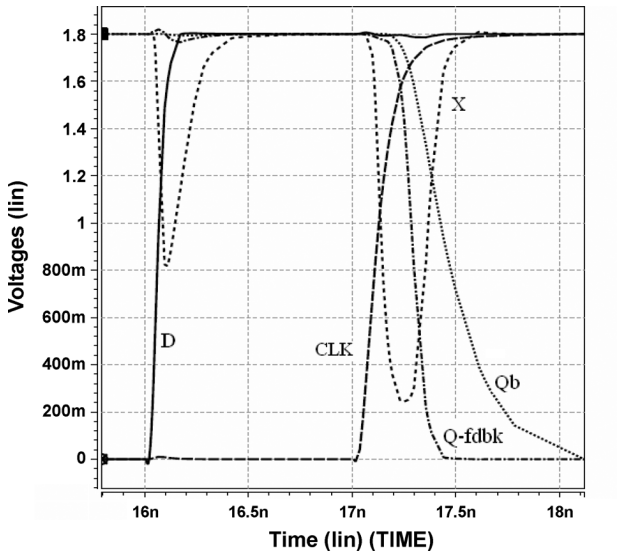

Fig. 12. D makes a $0->1$ transition.

four nodes (X, Y, X′, and Y′) switching redundantly at each clock rising edge and falling edge when D remains 1, without doing useful work. It also has a glitch at the output.

The ep-DSFF has only two gates in the critical path with a simple structure. However, it has an explicit pulse generator where two transmission gates have a current contention problem when the clock switches [25]. Furthermore, the exposed input diffusion of transmission gate TG3 makes ep-DSFF susceptible to noise [1], meanwhile the inverter I5 should be very weak to reduce fighting with incoming data input D for performance purposes. So one inverter could be placed before D feeds to the transmission gate (TG3) to improve robustness and driving ability, but the power and delay will degrade from those results in Table I. ep-DSFF has four clocked inverters as SPGFF does, but SPGFF has more redundant switching activity at X, Y, X′, and Y′ in addition to ten more transistors in total number and two more clocked transistors, so ep-DSFF has less power than SPGFF.

In view of power of all the designs, the newly proposed CBS_ip has the lowest power consumption. The low power consumption is due to four main factors. First, it has a clock branch sharing topology, where fewer transistors are clocked, which efficiently reduces the clock load. Second, the conditional discharge technique employed in the latch eliminates the redundant switching activity. Third, the split path technique reduces the short circuit current in the second stage. Fourth, an implicit pulse generator scheme with one inverter delay is used which further reduces power consumption.

In view of PDP, CBS_ip is comparable to ep-DSFF and better than SPGFF. However, ep-DSFF has a drawback of an exposed input diffusion subject to noise and a ratio concern. Standard cell latches are usually built with buffered inputs rather than exposed diffusion nodes [1]. If add one inverter at the input to avoid the exposed input diffusion, ep-DSFF's PDP will degrade. In addition, ep-DSFF uses an explicit pulse generator, so it can not be used with dynamic logic.

CBS_ip could work when D and CLK are using a low supply voltage, so it could be used as a level converting flip flop, similar to [31]and [32], to be placed where a low-voltage block meets a high-voltage block between pipeline stages in CVS systems. ep-DSFF cannot work with low swing clock.

Besides the typical condition (TT design corner), CBS_ip is simulated in the design corners of FF, SS, SF, and FS, it works correctly for all process corners.

Through simulation, we find that the power consumed by the always on pMOS P1 (including the short circuit current and the charging current to pull up node X to 1) is less than 5% of the total power consumption of the CBS_ip. Although P1 is always ON, short circuits only occur when D makes a transition of $0->1$. Then, Qb_fdbk disconnects the discharge path after two gate delays (turning off N7). After that, if D stays HIGH, the discharge path is already disconnected by N7; there would be no further short circuit. Essentially, the conditional discharge technique enables the use of pseudo-nMOS in this flip-flop. Pseudo-nMOS could be used in CDFF [31]and other flip-flops as well.

Table I shows the leakage power, CBS_ip has smaller leakage power since it has a high stack (five transistors). With feature size shrinking, the leakage current increases rapidly, the MTMOS technique could be used to reduce leakage power consumption [33]. Further, with technology scaling, process variation tolerant technique like combination of adaptive body bias and adaptive VDD may be used to improve functionality, performance of the die [34]. Reducing the variation of the optimal clock duty cycle from the symmetrical clock is important [25].

V. CONCLUSION

In this paper, we surveyed the double-edge clocking flip-flops and classified them into three groups. Conventional DEFF duplicate the latching component, hence duplicating the area and increasing the input loads. The explicit DE pulsed flip-flops have

an external pulse generator, so they have higher power consumption.

The newly proposed CBS_ip uses a clock branch sharing scheme to sample the clock transitions, which efficiently reduces the number of clocked transistors and results in lower power while maintaining a competitive speed. It employs the conditional discharge technique and the split path technique to reduce the redundant switching activity and short circuit current, respectively. The CBS_ip flip flop has the least number of clocked transistors and lowest power; hence, it is suitable for use in high-performance and low-power environments.

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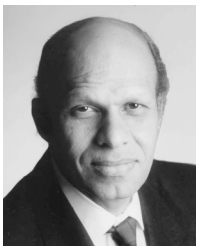

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