High-Performance and Low-Power Conditional Discharge Flip-Flop

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***Abstract*—In this paper, high-performance flip-flops are analyzed and classified into two categories: the conditional precharge and the conditional capture technologies. This classification is based on how to prevent or reduce the redundant internal switching activities. A new flip-flop is introduced: the conditional discharge flip-flop (CDFF). It is based on a new technology, known as the conditional discharge technology. This CDFF not only reduces the internal switching activities, but also generates less glitches at the output, while maintaining the negative setup time and small D-to-Q delay characteristics. With a data-switching activity of 37.5%, the proposed flip-flop can save up to 39% of the energy with the same speed as that for the fastest pulsed flip-flops.**

***Index Terms*—Digital CMOS, flip-flop, low power, very large scale integration (VLSI).**

I. Introduction

THE clock system, composed of the clock interconnection network and timing elements (flip-flops and latches), is one of the most power consuming components in a very large scale integration (VLSI) system. It accounts for 30%–60% of the total power dissipation in a system [1]. Moreover, in order to sustain the trend of higher performance and throughput, more timing elements will be employed for extensive pipelining of not only datapath sections, but also global bus interconnects, causing the power dissipation of the clock system to become more dominant. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed. In addition, from a timing perspective, flip-flop latency consumes a large portion of the cycle time while the operating frequency increases. Accordingly, flip-flop choice and design has a profound effect both in reducing the power dissipation and in providing more slack time for easier time budgeting in high-performance systems. These reasons are the main thrust for the increased interest in flip-flop design and analysis. A wide selection of different flip-flops can be found in the literature [1]–[18].

Many contemporary microprocessors selectively use master-slave and pulse-triggered flip-flops [2]. Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are characterized by their hard-edge property. Examples of master-slave flip-flops include the transmission gate based POWERPC 603 [3], push–pull D-type-flip-flop (DFF) [4], and true single phase clocked (TSPC) flip-flop [5]. Another edge-triggered flip-flop is the sense amplifier based flip-flop (SAFF) [6]. All these hard-edged flip-flops are characterized by positive setup time, causing large D-to-Q delays. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. The logic complexity and number of stages inside these pulse-triggered flip-flops are reduced, leading to small D-to-Q delays. One of the main advantages of pulse-triggered flip-flops is that they allow time borrowing across cycle boundaries as a result of the zero or even negative setup time. Due to these timing issues, pulse-triggered flip-flops provide higher performance than their master-slave counterparts, and since we are concerned about performance, master-slave flip-flops will not be discussed any further in this paper.

Pulse-triggered flip-flops can be classified into two types, implicit and explicit, and this classification is due to the pulse generators they use. In implicit-pulse triggered flip-flops (ip-FF), the pulse is generated inside the flip-flop, for example, hybrid latch flip-flip (HLFF) [7], semi-dynamic flip-flop (SDFF) [8], and implicit-pulsed data-close-to-output flip-flop (ip-DCO) [9] . Whereas, in explicit-pulse triggered flip-flops (ep-FF), the pulse is generated externally, for example, explicit-pulsed data-close-to-output flip-flop (ep-DCO) [9] and the flip-flops from [10] and [11].

At first glance, ep-FF consumes more energy due to the explicit pulse generator. However, ep-FF has several advantages. First, ep-FF can have the pulse generator shared by neighboring flip-flops, a technique that is not straightforward to use in ip-FF. This sharing can help in distributing the power overhead of the pulse generator across many ep-FF, and a system using ep-FF will be more energy efficient than a system using ip-FF. Second, double-edge triggering is straightforward to implement in ep-FF, but it is difficult to deploy in ip-FF. Using double-edge triggering, where data latching or sampling is issued at both the rising and falling edges, usually allows the clock routing network to consume less power. For example, for a system with a throughput of one operation per cycle and a clock frequency f, double-edge triggering results in two operations being executed in one cycle; if we use half the frequency, we can maintain the same throughput of the original system. With half the frequency, the clock switching activity is reduced by half, which leads to considerable power savings in the clock routing network. Third, ep-FF could have the advantage of better performance as the height of the nMOS stack in ep-FF is less than that in ip-FF [2]. With this rationale, the authors believe that ep-FF topology is more suited for low-power and high-performance designs.

One effective technique to obtain power savings inside a flip-flop can be devised by realizing the fact that a common

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property among various high-speed flip-flops is the utilization of dynamic structure. This dynamic behavior causes a lot of power to be wasted as a result of unnecessary internal switching activity, especially in moderate or lower data activity environments. Reducing these activities can effectively result in reducing the overall power dissipation. In this regard, several existing approaches to reduce the internal switching activity are surveyed and classified into conditional precharge and conditional capture techniques. This paper reviews these techniques with some associated flip-flops utilizing these techniques. Also, a new technique, Conditional Discharge, is proposed in this paper. This new technique not only reduces the internal switching activity of flip-flops but also overcomes the limitations associated with some of the techniques mentioned above.

This paper is organized as follows. Section II describes different techniques used to reduce the switching activity inside flip-flops, and it introduces the new technique. Section III describes the explicit pulse-triggered flip-flop, ep-DCO, and the associated limitations. Section IV presents the new flip-flop utilizing the new technique for low-power and high-speed designs. Section V compares flip-flops (ep-DCO and CDFF) and shows the simulation results. Finally, we conclude in Section VI.

II. Techniques for Reducing Switching Activity

Most of the flip-flops presented here are dynamic in nature, and some internal nodes are precharged and evaluated in each cycle without producing any useful activity at the output when the input is stable. Reducing this redundant switching activity has a profound effect in reducing the power dissipation, and in the literature many techniques were presented for this purpose [12]–[16]. A brief survey of such techniques is conducted in this work, and the main techniques were classified into: conditional precharge and conditional capture.

A. Conditional Precharge Technique

The general idea of this technique is that the precharging path is controlled to avoid precharging the internal node when D stays HIGH. Fig. 1 shows the general scheme of the conditional precharge technique. In the absence of the pMOS precharge control and when D stays HIGH for a long time, the discharge path will be on during the evaluation periods, causing node X to discharge after each precharging phase. To eliminate these charging/discharging activities, a pMOS transistor is inserted in the precharging path, which will prevent the precharging of node X in case the data input is stable HIGH. Flip-flops CPFF [12], DE-CPFF [13], and CP-SAFF [14] employ this technique; they are shown in Fig. 2(a)–(c) respectively. For example, in CP-FF and dual-edge clocking conditional precharge flip-flop (DE-CPFF) the control signal is Q whereas in conditional precharge sense-amplifier flip-flop (CP-SAFF) the control signal is the data input D.

B. Conditional Capture Technique

This technique is based on the clock-gating idea, and Fig. 3 shows the general scheme for this technique. This technique is mainly applied for implicit pulse-triggered flip-flops such as CCFF [15] and imCCFF [16] which are shown in Fig. 4(a) and (b), respectively. Essentially these two flip-flops employ the internal clock-gating approach. Flip-flops in this category feature a transparent window period that is used to sample the input. This window, created by an implicit pulse generator, is determined by the time when both clocked transistors in the first stage are simultaneously on. After sampling a HIGH state at the input, the output Q will be HIGH. This output state could be used to shut the transparent window as long as it is HIGH, preventing the redundant activities of the internal node X. In this technique, a Q-controlled gate is inserted on the path of the delayed clock to the first stage, Fig. 3.

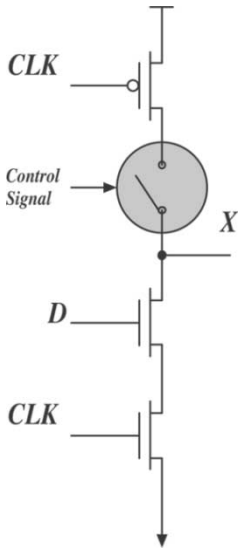

Fig. 1. Conditional precharge technique.

In Fig. 4, the condition captured flip-flop (CCFF) is introduced to reduce redundant power at the internal node. This flip-flop employs a scheme much like the JK-type-flip-flop [19], but it adds one more gate that is switching with the clock compared to HLFF [7]. This addition leads to an increase in the power consumed by the clock system, and it may offset the savings gained from reducing the internal redundant switching power. Moreover, employing the double-edge triggered technique will be complicated and the transistor count would increase because it requires the duplication of the NOR gate and other clocked transistors. A revised condition captured flip-flop (imCCFF), Fig. 4, is proposed to improve the energy-delay-product (EDP). A further enhancement on this flip-flop could be employed to reduce the switching activity on the internal node Y, which may further improve the EDP.

C. Proposed Conditional Discharge Technique

The clock-gating in the conditional capture technique results in redundant power consumed by the gate controlling the delivery of the delayed clock to the flip-flop. As a result, conditional precharge technique outperformed the conditional capture technique in reducing the flip-flop EDP [16]. But the conditional precharge technique has been applied only to ip-FF, and it is difficult to use a double-edge triggering mechanism for these flip-flops, as it will require a lot of transistors. A new technique, conditional discharge technique, is proposed in this paper for both implicit and explicit pulse-triggered flip-flops without

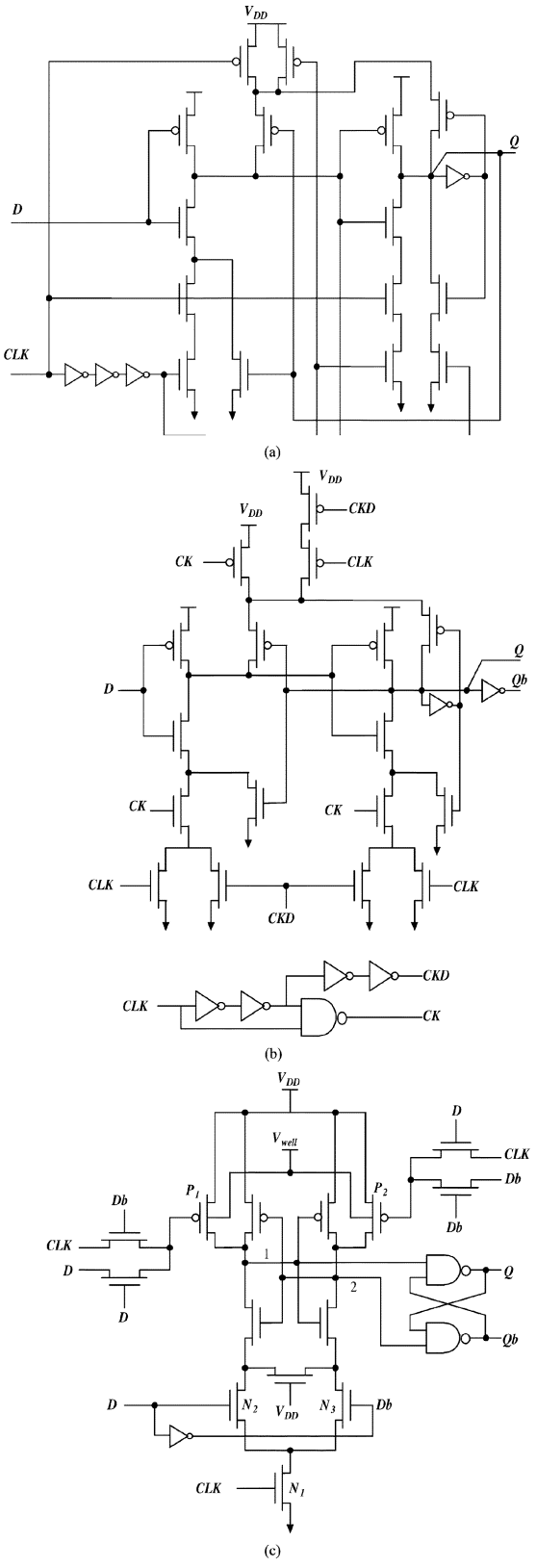

Fig. 2. Flip-flops using the conditional precharge technique. (a) CPFF. (b) DE-CPFF. (c) CP-SAFF.

the problems associated with the conditional capture technique, Fig. 5. Also, this new technique is employed to present a new flip-flop as well (Section IV). In this technique, the extra switching activity is eliminated by controlling the discharge

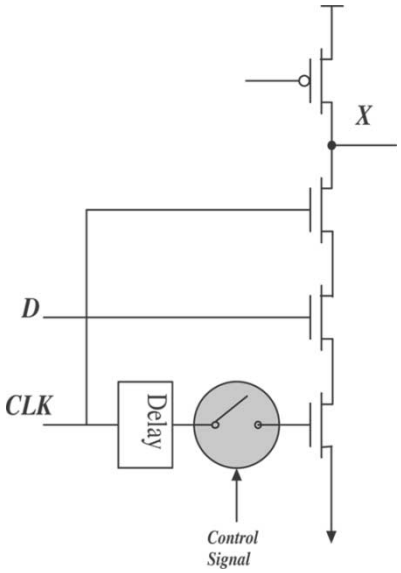

Fig. 3. Conditional capture technique.

path when the input is stable HIGH and, thus, the name Conditional Discharge Technique. In this scheme, an nMOS transistor controlled by Qb is inserted in the discharge path of the stage with the high-switching activity. When the input undergoes a LOW-to-HIGH transition, the output Q changes to HIGH and Qb to LOW. This transition at the output switches off the discharge path of the first stage to prevent it from discharging or doing evaluation in succeeding cycles as long as the input is stable HIGH.

III. Explicit Pulse-Triggered Flip-Flop

Pulse-triggered flip-flops outperform hard-edged flip-flops, as they provide a soft edge, negative setup time, and small D-to-Q delays, which help not only in reducing the delay penalty these flip-flops incur on cycle time but also help in absorbing the clock skew [7], [8], [20]. In general ep-FF do not offer any performance advantage over their ip-FF counterparts and consumes more energy due to the explicit pulse generator [9]. However, the pulse generator power dissipation overhead can be distributed among a group of flip-flops. Moreover, when double-edge triggered flip-flops are considered to reduce the power dissipation of the clock distribution network [21], the ep-FF is more suitable.

One example of ep-FF is the ep-DCO flip-flop; it is considered one of the fastest flip-flops due to its semi-dynamic structure [9]. It is well suited for very high-performance applications, where it can be employed in the most critical paths of a design to achieve a very small flip-flop delay. This allows more freedom in cycle budgeting especially with its negative setup time feature that is due to the use of the pulse triggering mechanism. Fig. 6 shows the schematic for the ep-DCO flip-flop; its semi-dynamic structure consists of two stages: a dynamic (first stage) and a static stage (second). After the rising edge of the clock, transistors $N2$ and $N3$ turn on for a short period of time, which is equal to the delay incurred by the pulse generator. During this period, the flip-flop is transparent and the input data propagates to the output. After the transparent period, the pull-down paths

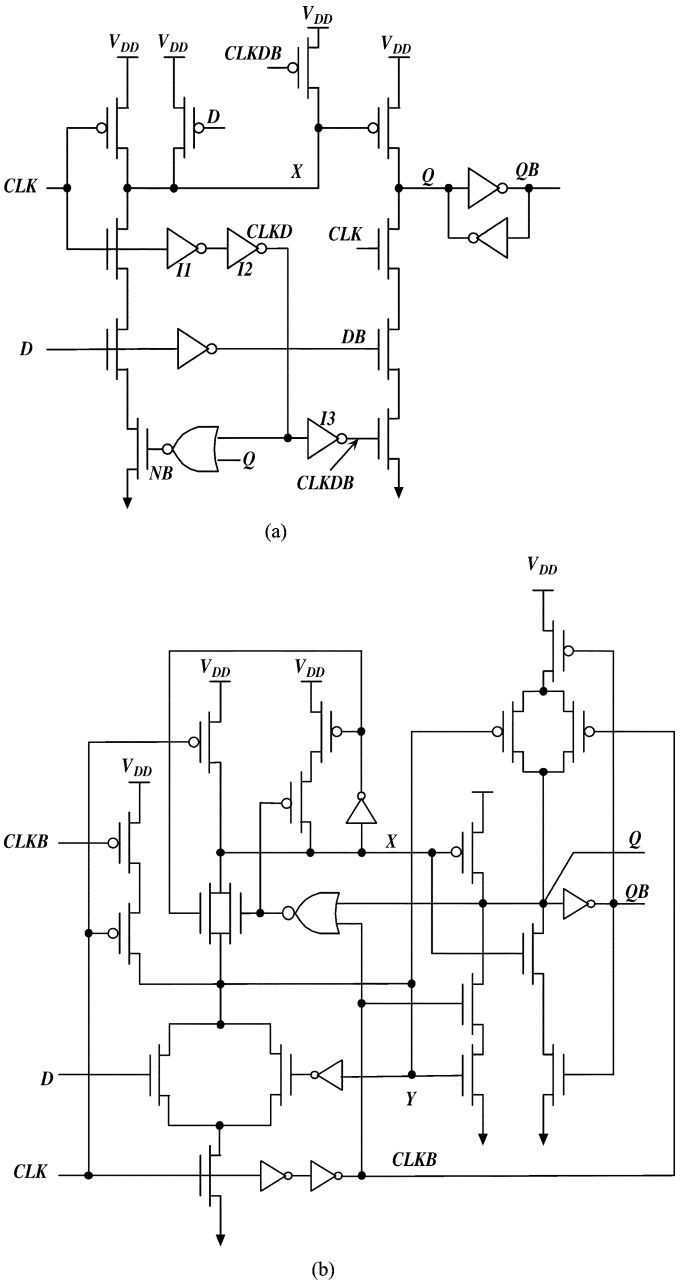

Fig. 4. Flip-flops using the conditional capture technique: (a) CCFF and (b) imCCFF.

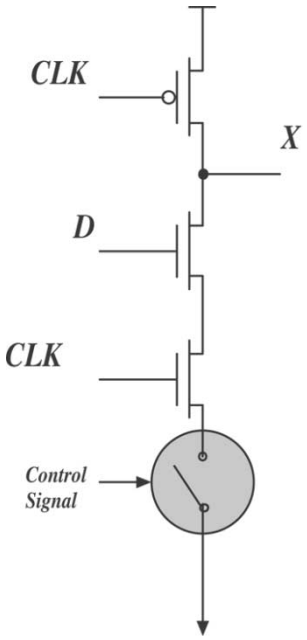

Fig. 5. Proposed conditional discharge technique.

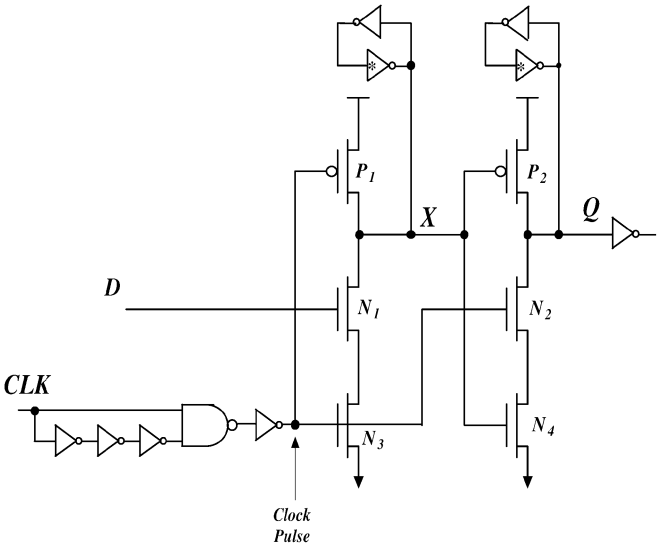

Fig. 6. Single-edge triggered explicit-pulsed flip-flop, ep-DCO.

in both stages are turned off via the same transistors $N2$ and $N3$. Hence any change at the input cannot pass to the output. Keepers are used to maintain the output and internal node states when the circuit is in the hold mode.

Careful analysis of the ep-DCO circuit reveals a significant amount of power being consumed by charging and discharging the internal node X. Node X is charged and discharged at every clock cycle, especially when the input D is not changing. Since these internal activities do not produce useful operation, the part of power dissipated during the charge/discharge events does not contribute to the circuit operation. Moreover, while the output is HIGH, the repeated charging/discharging of node X in each clock cycle causes glitches to appear at the output. As the , it creates a discharge path forinternal node X is precharged HIGH the output node that stays on for a small period of time after the start of the evaluation period [22]; this path causes the output to loose some of its charge. These glitches propagate to the driven gates not only to increase their switching power consumption but also to cause noise problems that may lead to system malfunctioning.

IV. Proposed Conditional Discharge Flip-Flop (CDFF)

The schematic diagram of the proposed flip-flop, conditional discharge flip-flop (CDFF), is shown in Fig. 7. It uses a pulse generator as in [9], which is suitable for double-edge sampling. The flip-flop is made up of two stages. Stage one is responsible for capturing the LOW-to-HIGH transition. If the input D is HIGH in the sampling window, the internal node X is discharged, assuming that (Q, Qb) were initially (LOW, HIGH) for the discharge

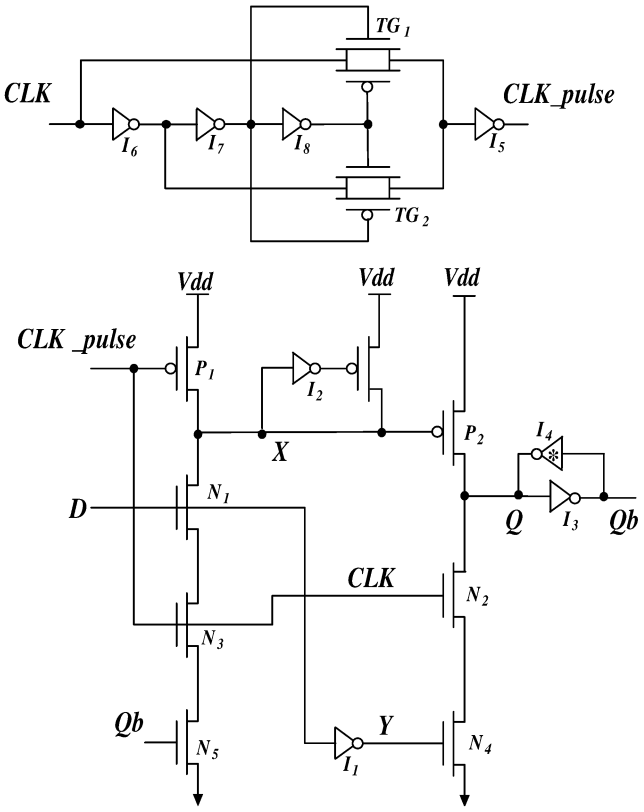

Fig. 7. Proposed conditional discharge double-edge triggered flip-flop, CDFF.

path to be enabled. As a result, the output node will be charged to HIGH through P2 in the second stage. Stage 2 captures the HIGH-to-LOW input transition. If the input D was LOW during the sampling period, then the first stage is disabled, and node X retains its precharge state. Whereas, node Y will be HIGH, and the discharge path in the second stage will be enabled in the sampling period, allowing the output node to discharge and to correctly capture the input data.

The conditional discharging scheme is employed in the CDFF as follows: in order to reduce the redundant switch power, we employ a discharge control transistor N5 at the discharge path of the first stage. When $Qb = \mathrm{HIGH}$, which means $Q = \mathrm{LOW}$ and $X = \mathrm{HIGH}$, N5 turns on, and the discharge path is enabled. If the input D makes a LOW-to-HIGH transition, and CLK_pulse is HIGH, N1, N5, and N3 switch on, the internal node X is discharged to LOW, and Q is pulled up to HIGH with Qb pulled down to LOW, which shuts off the nMOS stack in first stage. For this D transition (LOW-to-HIGH), X is discharged only once; i.e., consecutive HIGH level at D will not be sampled because the discharging path is inhibited by Qb. To ensure that the D HIGH-to-LOW transition is sampled by the flip-flop, dual path is used. Recall that the output rise transition tends to be the slow path (critical path); by employing dual path, capacity at node X is reduced, and thus the LOW-to-HIGH delay could be reduced.

Since node X is not charged and discharged every clock cycle, no glitches appear on the output node Q when the input D stays high, and Q will not be discharged at the beginning of each evaluation [22] as that in the other precharged dynamic circuits such as HLFF, SDFF, or ip-DCO. As a result, CDFF features less switching noise generation, which is an important

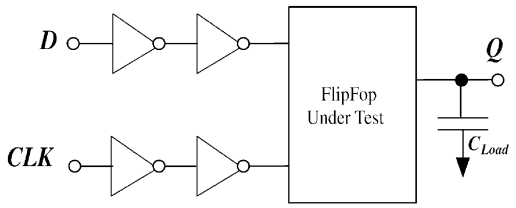

Fig. 8. Setup used for the flip-flops simulations. Inputs are driven by inverters, and the output is driving a load of 14 minimum inverters (FO14).

issue in mixed signal circuits. Moreover, node X stays HIGH or precharged in most cases, which helps in simplifying the keeper structure as shown in Fig. 7, and it also reduces the capacitive load at node X.

Double-edge triggered pulse generator [9] is utilized to further reduce power on the clock tree and the clocked transistors in pulse generator. Double-edge triggered flip-flops can have the same data throughput as the single-edge triggered flip-flops. The power saved in the clock distribution network is not included when we compare the power consumption. Also, clock-gating [23], [24] can be easily applied to eliminate power consumption when D keeps the same value. Although the input load is increased, the overall power saving could be achieved significantly.

V. Simulation Results

The simulation results for all flip-flops were obtained in a 0.18 μm CMOS technology at room temperature using HSPICE, the supply voltage is 1.8 V. The setup used in our simulations is shown in Fig. 8. In order to obtain accurate results, we have simulated the circuits in a real environment, which dictates that the flip-flops' inputs (clock, data) are driven by fixed input buffers, and the outputs are required to drive an output load. The value of the capacitance load at output node Q is selected to simulate a fan out of fourteen standard sized inverters (FO14) [19] for the technology in use. Assuming uniform data distribution, we have supplied the input D with 16-cycle pseudorandom input data with activity 37.5% to reflect the average power consumption. The input pattern "1010" represents maximum input switching act "1111" and "0000" represent zero switching activity. A clock frequency of 250 MHz is used for single-edge triggered flip-flops, whereas a 125-MHz frequency is used for double-edge triggered flip-flops.

For fair comparison, we present the energy versus delay and the EDP versus delay curves. Power consumed in data and clock drivers are included in our measurements. Circuits were optimized for minimum power delay product, PDP. The D-to-Q delay [20] is obtained by sweeping the LOW-to-HIGH and HIGH-to-LOW data transition times with respect to the clock edge, and the minimum data to output delay corresponding to optimum setup time is recorded. Minimum D-to-Q delay is an appropriate metrics for flip-flops because it reflects the correlations between D-to-Clock delay, Clock-to-Q delay, and the D-to-Q delay.

Fig. 9 shows the curve of energy-per-cycle at different minimum D-to-Q propagation delays for the flip-flops: ep-DCO and CDFF. We record the D-to-Q delay at every 10–20 ps

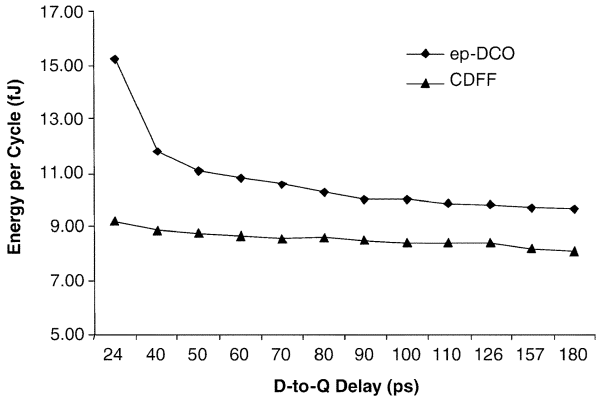

Fig. 9. Energy-per-cycle versus D-to-Q delay curves for ep-DCO and CDFF.

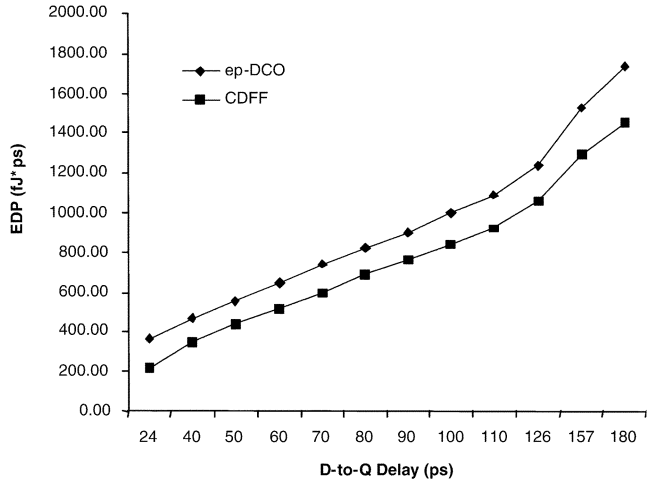

Fig. 10. EDP versus D-to-Q delay curves for ep-DCO and CDFF.

interval in the range 180 ps to 24 ps to plot the curve. The transistor sizes increase while the delay decreases. Energy is reduced in the case of CDFF by almost 20.5% at target D-to-Q delay of 65 ps and up to 39% at 24 ps. As the target delay decreases, the energy advantage of CDFF over ep-DCO increases. Fig. 10 shows the EDP curve as well. For smaller D-to-Q delays, CDFF achieves up to 39% improvements in EDP than ep-DCO. ep-DCO has more energy consumption due to the presence of redundant switching activity.

Figs. 11 and 12 show snapshots of the waveforms for the two flip-flops. The internal switching activity of CDFF at node X is less than that for ep-DCO. The waveforms show that the new flip-flop outputs are glitch-free when the input stays high.

In addition, Table I shows the simulation results of various flip-flops classified in Section II. In view of DQ delay, CDFF and ep-DCO have the smallest delay because ep-DCO has less nMOS stack height than implicit pulse-triggered flip-flops like CCFF and CPFF; CDFF uses dual path, which generally has better driving ability to help achieve small delay. CP-SAFF has large D-to-Q delay due to its hard edge characteristic and low swing clock.

In view of the power consumption, CDFF consumes the least, while ep-DCO and imCCFF consume more power since redundant switching activity exists at X and Y nodes in ep-DCO and imCCFF respectively.

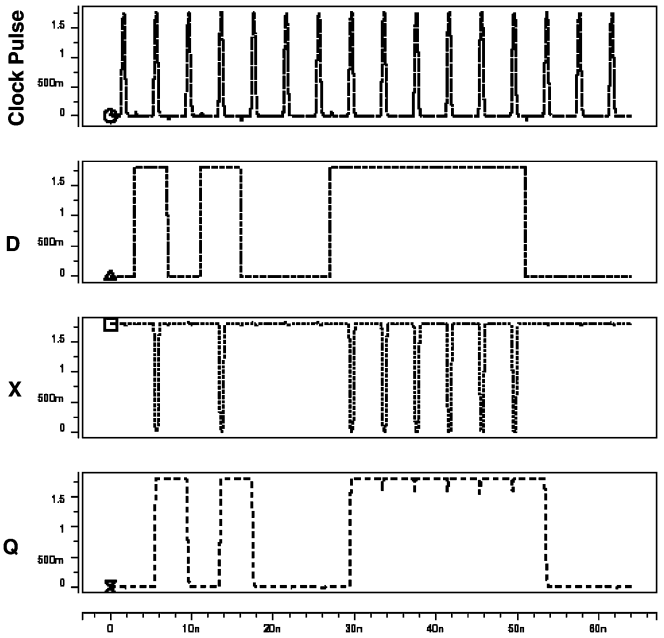

Fig. 11. Waveform for the ep-DCO flip-flop, lot of switching activities for X exist when D is stable HIGH. Also some associated glitches are apparent on the output Q.

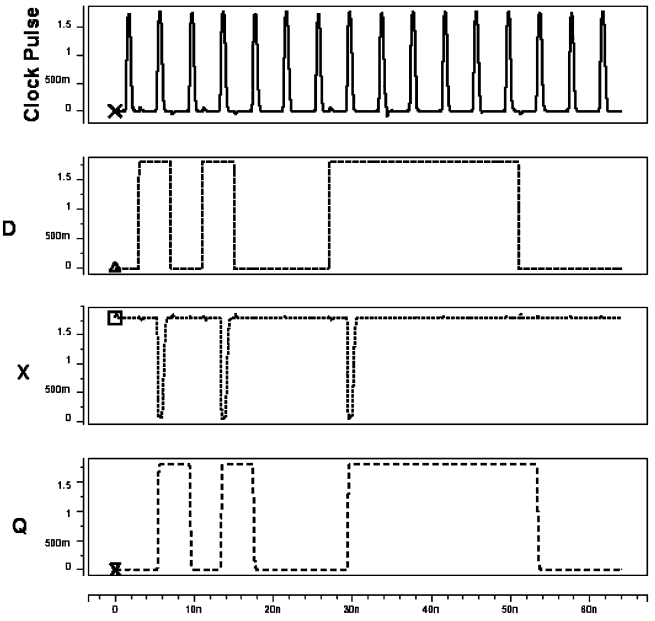

Fig. 12. Waveform for CDFF, switching activity at node X is reduced, without any glitches on the output Q.

TABLE I
COMPARING THE FLIP-FLOP CHARACTERISTICS AGAINST 6 OTHER FLIP-FLOPS IN TERMS OF DELAY, POWER, AND POWER DELAY PRODUCT

	# of Tr.	# of Clocked Tr.	DQ (ps)	P (uW)	PDP (fJ)
imCCFF	32	12	233	27.0	6.29
CCFF	26	13	206	22.6	4.66
SAFF_CP	24	3	545	21.8	11.88
DE-CPFF	33	21	226	21.6	4.88
CPFF	23	12	189.2	22.4	4.24
CDFF	28	15	185	20.2	3.74
ep-DCO	26	15	184	24.4	4.49

In view of PDP comparison, CDFF has the smallest PDP; SAFF-CP has the largest PDP because its relatively very large D-to-Q delay. Due to the complexity within CCFF and imCCFF, their PDP are larger than CDFF.

For low-voltage environment, these techniques could also be used. However, with threshold voltage scaling, the leakage power control is essential. Under 1.0 V, the proposed CDFF could be implemented with MTCMOS [25], dual-V_t [26] techniques to control leakage power consumption.

VI. Conclusion

In this paper, a new technique, conditional discharge, is introduced to reduce the switching activity of some internal nodes in flip-flops. This technique was utilized in a new flip-flop, conditional discharge flip-flop or CDFF. With a data switching activity of 37.5%, the new flip-flop can save up to 39% of the energy with the same speed as that for the fastest pulsed flip-flops. While ep-DCO is suitable for speed critical paths, CDFF is suitable for both speed critical paths and speed-insensitive paths for energy-efficiency. Moreover, in terms of PDP, CDFF outperforms the conditional capture flip-flops (CCFF, imCCFF) as well as conditional precharge flip-flops (CPFF, DE-CPFF). The above Conditional Discharge Technique could be applied to implicit pulsed flip-flops like ip-DCO and HLFF as well.

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References

[1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," *IEEE J. Solid-State Circuits*, vol. 33, pp. 807–811, May 1998.

[2] A. Chandrakasan, W. Bowhill, and F. Fox, *Design of High-Performance Microprocessor Circuits*, 1st ed. Piscataway, NJ: IEEE Press, 2001.

[3] G. Gerosa, "A 2.2 W, 80 MHz superscalar RISC microprocessor," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1440–1454, 1994.

[4] U. Ko and P. Balsara, "High-performance energy-efficient D-flip-flop circuits," *IEEE Trans. VLSI Syst.*, vol. 8, pp. 94–98, Feb. 2000.

[5] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, pp. 62–70, Feb. 1989.

[6] B. Nikolic, V. G. Oklobzija, V. Stojanovic, W. Jia, J. K. Chiu, and M. M. Leung, "Improved sense-amplifier-based flip-flop: Design and measurements," *IEEE J. Solid-State Circuits*, vol. 35, pp. 876–883, June 2000.

[7] H. Partovi, R. Burd, U. Salim, F. Weber, L. DiGregorio, and D. Draper, "Flow-through latch and edge-triggered flip-flop hybrid elements," in *Proc. Dig. ISSCC*, Feb. 1996, pp. 138–139.

[8] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R. Wang, A. Mehta, R. Heald, and G. Yee, "Semi-dynamic and dynamic flip-flops with embedded logic," in *Proc. Symp. VLSI Circuits, Dig. Tech. Papers*, June 1998, pp. 108–109.

[9] J. Tschanz, S. Narendra, Z. P. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered & dual edge-triggered pulsed flip-flops for high-performance microprocessors," in *Proc. ISPLED'01*, Huntington Beach, CA, Aug. 2001, pp. 207–212.

[10] S. Hesley *et al.*, "A 7th-generation X86 microprocessor," in *1999 IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1999, pp. 92–93.

[11] C. F. Webb *et al.*, "A 400-MHz S/390 microprocessor," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1665–1675, Nov. 1997.

[12] N. Nedovic and V. G. Oklobdzija, "Hybrid latch flip-flop with improved power efficiency," in *Proc. Symp. Integrated Circuits Systems Design, SBCCI2000*, Manaus, Brazil, Sept. 18–22, 2000, pp. 211–215.

[13] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in *Proc. Int. Symp. Low-Power Electronics . Design*, Monterey, CA, Aug. 12–14, 2002, pp. 56–59.

[14] Y. Zhang, H. Yang, and H. Wang, "Low clock-swing conditional-precharge flip-flop for more than 30% power reduction," *Electron. Lett.*, vol. 36, no. 9, pp. 785–786, Apr. 2000.

[15] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1263–1271, Aug. 2001.

[16] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional techniques for small power consumption flip-flops," in *Proc. 8th IEEE Int. Conf. Electronics, Circuits Systems*, Malta, Spain, Sept. 2–5, 2001, pp. 803–806.

[17] P. Zhao, T. Darwish, and M. Bayoumi, "Low power and high-speed explicit-pulsed flip-flops," in *Proc. 45th IEEE Int. Midwest Symp. Circuits Systems Conf.*, Tulsa, OK, Aug. 4–7, 2002.

[18] M. Tokumasu, H. Fujii, M. Ohta, T. Fuse, and A. Kameyama, "A new reduced clock-swing flip-flop: NAND-type keeper flip-flop (NDKFF)," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2002, pp. 129–132.

[19] V. G. Oklobdzija, "Clocking in multi-GHz environment," in *Proc. 23rd IEEE Int. Conf. Microelectronics*, vol. 2, 2002, pp. 561–568.

[20] V. Stojanovic and V. Oklobdzija, "Comparative analysis of master-slave latches and flip-flops for high-performance and low power system," *IEEE J. Solid-State Circuits*, vol. 34, pp. 536–548, Apr. 1999.

[21] E. Friedman, "Clock distribution networks in synchronous digital integrated circuits," *Proc. IEEE*, vol. 89, pp. 665–692, May 2001.

[22] J. Rabaey, *Digital Integrated Circuits*. Englewood Cliffs, NJ: Prentice-Hall, 1996.

[23] Q. Wu, M. Pedram, and X. Wu, "Clock-gating and its application to low power design of sequential circuits," *IEEE Trans. Circuits Syst. I*, vol. 47, pp. 415–420, Mar. 2000.

[24] Y. Xia and A. E. A. Almaini, "Differential CMOS edge-triggered flip-flop with clock-gating," *Electron. Lett.*, vol. 38, no. 1, pp. 9–11, Jan. 2002.

[25] S. Shigematsu, S. Mutoh, Y. Matsuya, Y. Tanabe, and J. Yamada, "A 1-V high speed MTCMOS circuit scheme for power-down applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 861–869, 1997.

[26] J. Tschanz, Y. Ye, L. Wei, V. Govindarajulu, N. Borkar, S. Burns, T. Karnik, S. Borkar, and V. De, "Design optimizations of a high performance microprocessor using combinations of dual-Vt allocation and transistor sizing," in *IEEE Symp. VLSI Circuits, Dig. Tech. Papers*, June 13–15, 2002, pp. 218–219.

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